12/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0013997790 - Drawing available
WPI ACC NO: 2004-178974/200417
XRPX Acc No: N2004-142285
Integrated circuit of microprocessor, includes standard chip-level test access port controller that stores core select bits, each indicating whether corresponding core is selected for built-in self test (BIST) operation
Patent Assignee: PENDURKAR R Y (PEND-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: PENDURKAR R Y
Patent Family (6 patents, 101 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20040006729	A1	20040108	US 2002189870	A	20020703	200417	B
WO 2004005949	A1	20040115	WO 2003US21101	A	20030702	200417	E
AU 2003249712	A1	20040123	AU 2003249712	A	20030702	200459	E
GB 2404446	A	20050202	WO 2003US21101	A	20030702	200510	E
			GB 200425535	A	20041119		
TW 225199	B1	20041211	TW 2003118226	A	20030703	200535	E
TW 200405166	A	20040401	TW 2003118226	A	20030703	200568	E

Priority Applications (no., kind, date): US 2002189870 A 20020703

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040006729	A1	EN	15	8	
WO 2004005949	A1	EN			

National Designated States, Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Regional Designated States, Original: AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

AU 2003249712	A1	EN	Based on CPI patent WO 2004005949
GB 2404446	A	EN	PCT Application WO 2003US21101 Based on CPI patent WO 2004005949
TW 225199	B1	ZH	
TW 200405166	A	ZH	

Alerting Abstract US A1
NOVELTY - The circuit comprises memory elements, core-level master BIST (built-in self test) controller (304) and standard core-level **test access port (TAP) controller** (302), integrally coupled to **each** other. A standard chip-level **test access port controller** coupled to chip-level master BIST controller, has a core select **register** for storing core select bits, each indicating whether a corresponding core is selected for a BIST operation.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following :

1. built-in self test (BIST) operation method; and

2. multi-core chip.

USE - Integrated circuit for use in microprocessor.
ADVANTAGE - Allows numerous pre-existing processor cores replicated on multi-core chip (MCC) to be tested using standard chip level test architectures using without altering the design of individual core architectures. Hence, fabrication of the MCC can be performed without incurring time and expense required to develop and verify a new or modified design.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the multi-core chip.
300 multi-core chip
302 TAP controller
304 master BIST controller
308(1)-308(n) cores

19/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0016192072 - Drawing available
WPI ACC NO: 2006-723713/200675
XRPX Acc No: N2006-568556
Joint test action group test access port controller nesting method, involves selecting available bit from selectable bit register of host joint test action group test access port controller, where register has available bits
Patent Assignee: XILINX INC (XILI-N)
Inventor: SCHULTZ D P
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 7111217 B1 20060919 US 200286129 A 20020228 200675 B

Priority Applications (no., kind, date): US 200286129 A 20020228

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 7111217 B1 EN 12 3

Alerting Abstract US B1
NOVELTY - The method involves selecting an internal protocol (IP) core joint test action group test access port (JTAG TAP) controller to be coupled in series with a host JTAG TAP controller. An available bit is selected from a selectable bit register of the controller, where the bit register has available bits. An apparent length of an instruction register of the controller is extended by using the available bit from the selectable bit register.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1. a method for ensuring an information register length for nested joint test action group test access port controllers for IP cores;

2. a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC;

3. a system for performing boundary scan functions on IP cores.

USE - Used for nesting a joint test action group test access port (JTAG) controller.
ADVANTAGE - The selectable bit register provides flexibility in the joint test action group test access port architecture by permitting selection of various register sizes to accommodate the IP cores.
DESCRIPTION OF DRAWINGS - The drawing shows a representation of a flexible configuration for nesting joint test action group test access port controllers.